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SYSTEM FOR CONTROLLING INTERNATIONAL MOBILE TELECOMMUNICATIONS - 2000 (IMT-2000) BASE STATION

Field of the Invention

The present invention relates to a telecommunication system; and, more particularly, to a base transceiver station (BTS) interface subsystem (BIS) for use in an international mobile telecommunication - 2000 (IMT-2000) base station controller.

Description of the prior Art

An international mobile telecommunications - 2000 (IMT-2000) system transmits various kinds of traffic data by employing an asynchronous transfer mode (ATM) scheme.

Fig. 1 is a schematic diagram showing a typical IMT-2000 base station controller.

Referring to Fig. 1, the typical IMT-2000 base station controller includes an IMT-2000 base transceiver station (BTS) 10, a BTS interface subsystem (BIS) 20, an ATM switch 30, an ATM multiplexing subsystem (AMS) 40, a selection/distribution subsystem (SDS) 50 and a mobile services switching center (MSC) 60. The typical IMT-200 base station controller further includes a controller/signaling subsystem (CSS) 70 and a base station management subsystem (BEMS) 80.

The BIS 20 performs an interface with the BTS 10, and the

ATM switch 30 switches the ATM cells that are transmitted from the BIS 20. The AMS 40 performs an interface between the ATM switch 30 and the MSC 60, and the SDS 50 performs an operation of transcoding sound traffic data of ATM cell type. The CSS 70 manages wireless resources, a call control and the like, and the BEMS 80 entirely manages operations related to the base station and the controller.

The BIS 20 includes four ATM frame/deframe assemblies (AFDAs) 21 to 24 and an ATM multiplexing/demultiplexing assembly (AMDA) 25. Each AFDA 21 to 24 divides the ATM cells transmitted from the BTS 10 into ATM adaptation layer 2(AAL2) ATM cells and AAL5 ATM cells. The AMDA 25 multiplexes the ATM cells transmitted from the AFDAs 21 to 24 to transmit multiplexed ATM cells to the ATM switch 30. Furthermore, the AMDA 25 demultiplexes the ATM cells transmitted from the ATM switch 30 to transmit demultiplexed ATM cells to the AFDA 21 to 24.

The AMS 40 includes a first selector multiplexer/demultiplexer (SMDA) 41, a second SMDA 42 and a plurality of selector/transcode interface assemblies (STIAs) 45 to 48.

The first SMDA 41 demultiplexes ATM cells transmitted from the ATM switch 30, and multiplexes ATM cells transmitted through a cell bus and then transmits multiplexed ATM cells to the ATM switch 30.

The second SMDA 42 multiplexes/demultiplexes ATM cells transmitted from the MSC 60.

The plurality of the STIAs 45 to 48 checks what kind of the ATM cells, which are transmitted from the first and the second SMDA 41 and 42, are. Then, the STIAs transmit AAL2 ATM cells of sound data to the SDS 50.

The SDS 50 includes a STIA 51 for interfacing with the AMS 40 and a selector/transcode board assembly (STBA) 52 for transcoding the sound data transmitted from the STIA 51.

Fig. 2 is a block diagram illustrating an AFDA shown in Fig. 1.

Referring to Fig. 2, each of four AFDAs 21 to 24 includes four E1 line interface units (LIUs) 200 to 203, four universal test and operations physical interface for ATM (UTOPIA) function execution units 204 to 207, four type conversion units 208 to 211, a 4:1 multiplexer 212 and a cell bus interface unit 213.

Each of the LIUs 200 to 203 performs an ATM physical layer function and interfaces with an E1 line coupled to the BTS 201.

Each of the UTOPIA function execution units 204 to 207, respectively coupled to the LIUs 200 and 203, interfaces with UTOPIA level 1.

Each of the type conversion units 208 to 211 performs a type conversion of ATM cells in order to allow the ATM cell to be ATM-switchable, and converts ATM-switched ATM cells into AAL2 ATM cells.

The 4:1 multiplexer 212 multiplexes the ATM cells transmitted from the type conversion units 208 to 211 to

transmit multiplexed ATM cells to the cell bus interface unit 213. Furthermore, the 4:1 multiplexer 212 demultiplexes the ATM cells transmitted from the cell bus interface unit 213 to transmit demultiplexed ATM cells to the type conversion units 208 to 211.

The cell bus interface unit 213 transmits the ATM cells, which are transmitted from the 4:1 multiplexer 212, to the AMDA 25 through an interface with the cell bus, and it also receives the ATM cells transmitted from the AMDA 25.

Fig. 3 is a block diagram showing the AMDA 25 shown in Fig. 1.

Referring to Fig. 3, the AMDA 25 includes a processor 300, a 8 bit cell routing unit 301, a 8 bit multiplexer 302, a layer conversion unit 303 and two 8 bit user-network interface (UNI) units 304 and 305.

The processor, e.g., MPC860 supplied by Motorola, 300 performs an AAL5 process with respect to the ATM cells. The 8 bit cell routing unit 301 performs a routing of the ATM cells transmitted via the cell bus.

The 8 bit multiplexer 302 classifies the ATM cells transmitted from the 8 bit cell routing unit 301 into ATM cells to be transmitted to the processor 300 and ATM cells to be transmitted to the ATM switch 30. The layer conversion unit 303 performs an operation of an ATM layer conversion so that the processor 300 performs an AAL5 process with respect to the ATM cells transmitted from the 8 bit multiplexer 302.

The 8 bit UNIs 304 and 305 act as an interface between

the 8 bit multiplexer 302 and the ATM switch 30 at a speed of 155 Mbps.

Hereinafter, an operation of the typical IMT-2000 base station controller will be described with reference to Figs. 1 to 3.

Each LIU 200 to 203 contained in each AFDA 21 to 24 includes PM4313 chip, PM7344 chip, and a microprocessor such as MPC860. The PM4313 chip and PM7344 chip are provided by PMC-Sierra. The PM4313 chip for an electrical interface with the E1 line performs a line encoding/decoding function and processes four E1 lines. The PM7344 chip performs a multiplexing/demultiplexing function with respect to four E1 lines. The MPC860 stores the ATM cells outputted from the PM7344 and processes control signals.

The ATM cells transmitted from the BTS 10 via the E1 line are inputted through the PM4313 chip and the PM7344 chip to the MPC860, and then, transmitted to the UTOPIA function execution units 204 to 207. The UTOPIA function execution units 204 to 207 perform an interface to UTOPIA level 1 and transmit the ATM cells to the type conversion units 208 to 211. The type conversion units 208 to 211 performs a type conversion operation with respect to the ATM cells in order to allow the ATM cells to be switchable and then transmit the ATM cells to the 4:1 multiplexer 212. The ATM cells are transmitted to the AMDA 25 via the cell bus interface unit 213.

Then, the AMDA 25 multiplexes the ATM cells outputted from four AFDAs 21 to 24 to transmit multiplexed ATM cells to

the ATM switch 30. The ATM switch 30 routes the ATM cells and routed ATM cells are transmitted to the AMS 40. The AMS 40 transmits ATM cells corresponding to sound data to the SDS 50 and remaining ATM cells to the MSC 70, respectively.

In such a typical BIS, however, the conversion of ATM cell types is carried out in four AFDA, and the interface between the AMDA and the ATM switch is performed so that main control function is distributed. Therefore, there are disadvantages that an unnecessary function such as the cell bus interface is repeated. Furthermore, since each LIU contained in the AFDA includes the type conversion unit, there is a problem that a chip size is increased.

Summary of the Invention

It is, therefore, an object of the present invention to provide a BTS interface subsystem (BIS) for use in an international mobile telecommunication - 2000 (IMT-2000) base station controller.

In accordance with an aspect of the present invention, there is provided a system for controlling an international mobile telecommunications - 2000 (IMT-2000) base station, comprising: a base transceiver station (BTS) for providing asynchronous transfer mode (ATM) cells; an asynchronous transfer mode (ATM) switch for performing a switching of the ATM cells; and a BTS interface subsystem (BIS) for interfacing the base transceiver station (BTS) with the asynchronous

transfer mode (ATM) switch, wherein the BTS interface subsystem (BIS) includes a plurality of assembly symbol subsystems (ASSs) for receiving the ATM cells transmitted from the base transceiver station (BTS) and performing a type conversion of the ATM cells to output a type converted ATM cells to the asynchronous transfer mode (ATM) switch.

Brief Description of the Drawings

Other objects and aspects of the invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram showing a typical IMT-2000 base station controller;

Fig. 2 is a block diagram illustrating an AFDA shown in Fig. 1;

Fig. 3 is a block diagram showing an AMDA shown in Fig. 1;

Fig. 4 is a block diagram illustrating an IMT-2000 base station controller in accordance with the present invention; and

Fig. 5 is a block diagram illustrating an ASS shown in Fig. 4.

Detailed Description of the Preferred Embodiments

Fig.4 is a block diagram illustrating an IMT-2000 base

station controller containing a BIS in accordance with the present invention.

Referring to Fig. 4, the BIS 410 in accordance to the present invention includes assembly symbol subsystems (ASSs) 411 to 414. Each of the ASSs 411 to 414 performs a type conversion of ATM cells transmitted from a BTS 400 via E1 line in order to allow the ATM cells to be ATM-switchable, and interfaces with an ATM switch 420. At this time, the number of the ASSs is determined by that of the E1 lines.

Fig. 5 is a block diagram illustrating the ASS shown in Fig. 4.

Referring to Fig. 5, each of the ASSs 411 to 414 includes a processor 512 for controlling an operation of the BIS 410, a plurality of E1 interface units 500 to 503, a plurality of ATM physical layer execution units 504 to 507, a reception (RX) type conversion unit 508, a reception (RX) multiplexer 509, a transmission (TX) multiplexer 510, a transmission (TX) type conversion unit 511, a physical layer execution unit 513, and an optical transceiver 514.

The E1 interface units 500 to 503 restore and encode data transmitted via E1 lines and output E1 frame data.

The ATM physical layer execution units 504 to 507 extract ATM cells from the E1 frame data and perform an error correction operation to the ATM cell header and a cell rate decoupling operation. Furthermore, the ATM physical layer execution units 504 to 507 transmit data to the BTS 400.

The RX multiplexer 509 transmits ATM cells corresponding

to internal signals to the processor 512 and the remaining ATM cells to the RX type conversion unit 508.

The RX type conversion unit 508 classifies the ATM cells transmitted from the RX multiplexer 509 into AAL5 ATM cells and AAL2 ATM cells. At this time, the RX type conversion unit 508 bypasses the AAL5 ATM cells to the RX multiplexer 509, and converts the AAL2 ATM cells into AAL2 prime ATM cells to transmit the AAL2 prime ATM cells to the RX multiplexer 509.

The TX multiplexer 510 transmits ATM cells corresponding to the internal signals to the processor 512 and transmits the remaining ATM cells to the TX type conversion unit 511.

The TX type conversion unit 511 classifies the ATM cells transmitted from the TX multiplexer 510 into AAL5 ATM cells and AAL2 ATM cells. At this time, the TX type conversion unit 511 bypasses the AAL5 ATM cells to the TX multiplexer 510, and converts the AAL2 ATM cells into AAL2 prime ATM cells and transmits the AAL2 prime ATM cells to the RX multiplexer 509.

The physical layer execution unit 513 performs a physical layer function to the ATM cells at a speed of 155 Mbps, wherein the ATM cells are transmitted between the RX multiplexer 509 and the optical transceiver 514.

The optical transceiver 514 receives data from the physical layer execution unit 513 and transmits it to the ATM switch 420. Also, the optical transceiver 514 receives data from the ATM switch 420 and transmits it to the physical layer execution unit 513.

At this time, the number of the E1 interface units is

determined by a total number of the E1 lines that are controlled by the ASS. Each E1 interface unit can controls four E1 lines.

Each of the E1 interface units 500 to 503 includes PM4313 chip, and each of the ATM physical layer execution units 504 to 507 includes PM7344 chip. Furthermore, the physical layer execution unit 513 includes PM5346 chip.

Hereinafter, an operation of the BIS 410 contained in the IMT-2000 base station controller will be described in detail.

First, an interface function of the BIS 410 will be described in case where the ATM cells are transmitted from the BTS 400 to the ATM switch 420.

When the E1 interface units 500 to 503 receives the ATM cells from the BTS 400 via four E1 lines, the E1 interface units 500 to 503 performs data restoration/encoding functions and transmit E1 frame data to the ATM physical layer execution units 504 to 507. Then, the ATM physical layer execution units 504 to 507 extract ATM cells from the E1 frame data and perform an error correction operation to the ATM cell header and a cell rate decoupling operation.

The RX multiplexer 509 receives extracted ATM cells and classifies the extracted ATM cells. At this time, the RX multiplexer 509 transmits ATM cells corresponding to internal signals to the processor 512, and transmits the remaining ATM cells to the RX type conversion unit 508, respectively.

The RX type conversion unit 508 classifies the received ATM cells into AAL2 ATM cells and AAL5 ATM cells. At this time,

while the AAL5 ATM cells are bypassed to the RX multiplexer 509, the AAL2 ATM cells are converted into AAL2 prime ATM cells which are ATM-switchable. Here, the AAL2 prime ATM cells are made by extracting multi-user sound data on the AAL2 ATM cells according to the users. That is, the AAL2 prime ATM cells can be ATM-switchable. The AAL2 prime ATM cells are again transmitted to the RX multiplexer 509.

The RX multiplexer 509 transmits the received ATM cells to the physical layer execution unit 514 at a speed of 155 Mbps, and the physical layer execution unit 513 transmits the ATM cells to the ATM switch 420 via the optical transceiver 514.

Second, an interface function of the BIS 400 will be described in case where the ATM cells are transmitted from the ATM switch 420 to the BTS 400.

ATM cells are transmitted from the ATM switch 420 to the physical layer execution unit 513 via the optical transceiver 514, and the physical layer execution unit 513 then transmits the ATM cells to the TX multiplexer 510. At this time, ATM cells of the internal control signals are transmitted to the processor 512 and the remaining ATM cells are transmitted to the TX type conversion unit 511.

Then, in the TX type conversion unit 511, the AAL5 ATM cells among the ATM cells are bypassed to the TX multiplexer 510. The ALL2 prime ATM cells are converted into the AAL2 ATM cells, and the AAL2 ATM cells are then transmitted to the TX multiplexer 510. The TX multiplexer 510 demultiplexes the ATM

cells, transmitted from the TX type conversion unit 511, to the ATM physical layer execution units 504 to 507. The ATM cells are then transmitted to the BTS 400 via corresponding ATM physical layer execution unit and corresponding E1 interface unit.

As described above, by implementing a plurality of ASS units for performing the ATM cell type conversion function and the ATM switch interface function, the main control function of the BIS is integrated so that an unnecessarily repeated function is effectively prevented.

While the present invention has been described with respect to certain preferred embodiments only, other modifications and variation may be made without departing from the spirit and scope of the present invention as set forth in the following claims.